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Power Quality Improvement Using Utt Based Unified Power Quality Conditioner (Upqc)

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Abstract— The purpose of this research is to evaluate the function of a Unified Power Quality Conditioner (UPQC) in a system of distribution that includes three wires and three different stages. The UPQC is a noteworthy example of a tailored power solution that is capable of efficiently addressing load balancing, the adjustment of power factors, and the suppression of current and voltage harmonics. The system is able to handle a broad variety of load configurations, including linear, inconsistent, and oscillating loads in any combination. Acquiring the reference signals for each and every one of the active electrical power filters in the series and the active power filters in the shunt requires the use of the unit template technique, abbreviated as UTT. The filters that have been constructed make use of a pair of proportional-integral (PI) controllers that are closed-loop. The arrangement of a shunt controller (SHUC) and a series controller (SERC) is part of the layout of a three-phase three-wire UPQC (UPQC). This study examined the progression of control systems and procedures for UPQC in order to boost power quality and design a flexible control strategy for improved UPQC performance. This research focuses on enhancing the efficiency and cost-effectiveness of UPQC. The control system that has been developed demonstrates improved steady-state and dynamic responsiveness, as seen by the simulation results conducted using MATLAB/Simulink. These results provide empirical support for the effectiveness of the UPQC.

Keywords— Harmonics; SPS MATLAB/SIMULINK; Load Balancing; UPQC-L; Power Quality; Voltage dip, Power Factor Correction.

I. INTRODUCTION

The growing usage of loads that aren't linear will inevitably lead to problems with the power quality. These problems are unavoidable. Single-phase loads make up a significant fraction of harmonic sources. These loads include laptops, neon compact lights, printers, printing equipment, and other electronic gadgets that are often found in household and business settings. In addition, it is important to point out that the efficiency of the loads has a tendency to be less than ideal. However, it is important to note that contemporary home and commercial equipment exhibit a high degree of sensitivity towards power quality issues. Historically, the highlighted power quality concerns were dealing with by utilisation of standard passive filters. However, the presence of certain constraints, examples of fixed adjustments and resonant with the source impedance may be seen in several academic studies, and the challenges associated with adjusting the time dependency of filter constraints, has prompted the requirement for hybrid and active filters. The UPQC is considered a significant bespoke power device that effectively addresses both current and voltage-related concerns concurrently. In the field of construction, it may be observed that a UPQC has resemblance to a UPFC. In both the UPQC and UPFC designs, two VSIs are linked together to a single dc battery. Transmission systems often use UPFCs, whereas distribution networks typically make use of UPQCs. These devices are utilized to concurrently execute shunt and series compensation. Nevertheless, it is worth noting that a UPFC primarily requires balancing shunt and/or series compensation. This is due to the fact that power transmission systems often function within a state of equilibrium and little distortion. Conversely, a power distribution system has the potential to exhibit direct current (DC) components, distortion, as well as imbalances in both voltages and currents. Hence, it is imperative for a UPQC to function well within this specific operational setting, whereby it carries out shunts or/and series compensation. The main goal of a UPQC is to mitigate power quality turbulences in the supply voltage, including sags, swells, imbalance, flicker, and harmonics. Additionally, the UPQC aims to address power quality concerns related to load current, including unbalance, reactive current, neutral current, and harmonics. Figure 1 is a schematic illustration of the UPQC scheme setup. The fundamental elements of this scheme are outlined below.

- The system employs a pair of inverters, one of which is linked in series through the line and operates as a series APF, while the other is attached thoughout the load and functions as a shunt APF.
- To link the shunt inverter and the network, a shunt coupling inductor, designated as LSh, is used. Additionally, it aids in the process of achieving a more uniform waveform. In certain cases, an isolation transformer is employed to achieve electrical isolation between the inverter and the network.
- A frequently employed direct current (DC) connection may be established through the utilization of either a capacitor or an inductor. Figure 1 illustrates the implementation of the direct current (dc) link, whereby a capacitor is employed to provide interconnection between the two inverters while simultaneously ensuring a consistent and self-sustaining dc bus voltage across the capacitor.
- The LC filter functions as a passive LPF and assists in lowering waves in the output voltage of the inverter caused by high-frequency switching.
- • In order to establish a relationship the series inverter to the networks, a series injection transformer is needed. A common method for choosing the right turn ratio is to decrease the voltage or current capacity of the series inverter.

Based on the UPQC Configuration, it may be categorized into two components: (a) Left Shunt UPQC-L and (b) Right Shunt UPQC-R. Since both inverters are linked in a back-to-back configuration, the categorization of the UPQC-R is decided by the relative placement of the shunt inverter in reference to the series inverter. This is because both inverters are connected in parallel. The shunt inverter has the capability to be positioned on either the right side, resulting in the designation of right shunt UPQC (UPQC-R), or on the left side, leading to the designation of left shunt UPQC (UPQC-L), in relation to the series inverter. Figure 1 depicts the system configuration of the UPQC- Left (UPQC-L), whereas Figure 2 illustrates the setup of the UPQC- Right (UPQC-R). The UPQC-R configuration is frequently employed among two setups. Regardless of the type of the load current acting on the system, the current(s) traveling across the series transformer in the UPQC-R system display largely sinusoidal characteristic. This is true as long as the shunt inverter properly compensates for current harmonics, reactive current, imbalance, and other related factors. Therefore, it can be concluded that UPQC-R exhibits superior overall performance in comparison to UPQC-L. The UPQC-L arrangement is occasionally employed in specific scenarios, such as mitigating the potential interference that may arise amid the passive filters and shunt inverter. This research focuses on enhancing the performance of UPQC-L in comparison to UPQC-R. This article also examines the decrease in cost and size of UPQC-L in comparison to UPQC-R, as evidenced by the ratings provided in the appendix section.

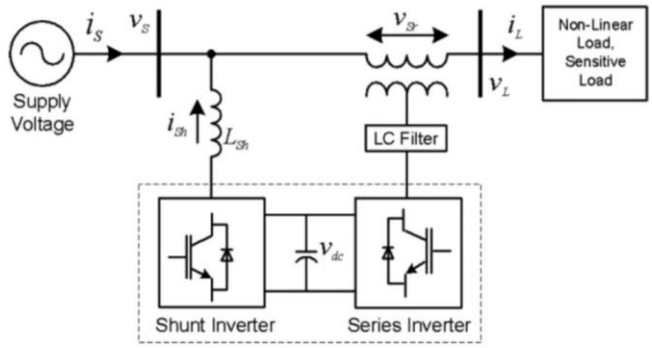

Fig. 1. UPQC-L system configuration

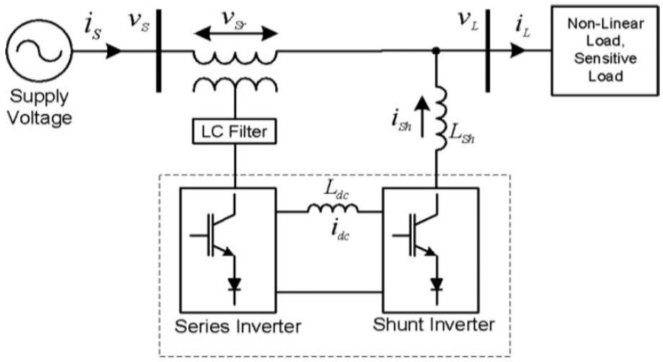

Fig. 2. UPQC-R block diagram representation.

II. SYSTEM CONFIGURATION

The system being discussed is seen in Figure 3. The UPQC is strategically installed upstream of the load in order to safeguard it against voltage-related distortions. Additionally, the UPQC checks to make ensure that the currents that are emanating from the sources are evenly distributed, sinusoidal, and in step with the source voltages. A three-phase rectifier might be connected to an R-L load in order to make adjustments to voltage and harmonics that are out of balance. A voltage drop is caused in the source voltage whenever the load component of an induction motor is abruptly linked to the source side.

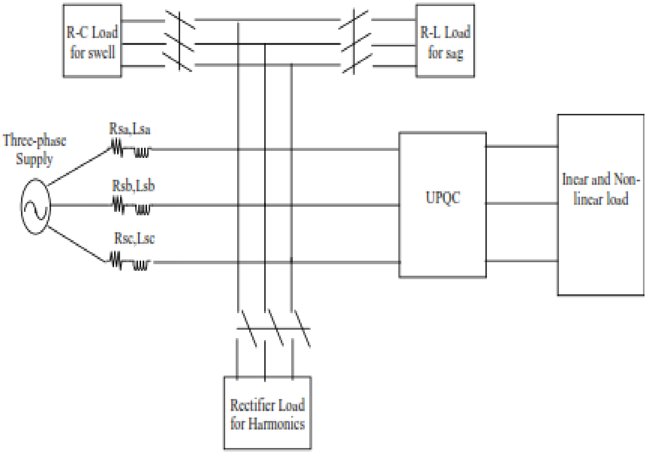

Fig.3 System under consideration

In order to realize the UPQC, two VSIs are utilized, connected in series with a shared DC link voltage. The second VSI acts as a series APF, while the first VSI acts as a shunt APF. Both VSIs are associated in parallel. Insulated Gate Bipolar Transistors (IGBTs) are used to construct a total of six switches that are used by each and every APF. Currents (i_{sa}, i_{sb}, and i_{sc}) are used to express the source current, currents (i_{la}, i_{lb}, and i_{lc}) are used to indicate the load current, and currents (i_{fa}, i_{fb}, and i_{fc}) are used to indicate the shunt APF currents in phase a, b, and c respectively. The voltages that are introduced by the series APF across phase a, b, and c, correspondingly, are abbreviated as (v_{inja}), (v_{injb}), and (v_{injc}), which are the shorthand symbols for the voltages. The efficacy of UPQC is evaluated using a load that is a mix of both non-linear and linear loads, which is the considered load. As an alternative to linear loads such as three-phase R-L loads, non-linear loads may be represented using a three-phase diode bridge rectifiers that have a resistive load on the dc side. In the appendix, you can find the measurements for the various constraints and loads associated with the circuit.

I. UPQC CONTROL STRATEGY

In order to provide signals as a reference to both the series and shunt APFs which are contained within the UPQC, the suggested control strategy's primary objective is to be implemented. While the control strategy for the series APF makes use of a method that is dependent on UTT, the control mechanism for the shunt APF making use of two closed-circuit PI controllers. The control technique for the series APF is described further below. The UTT approach is used in the control approach for the series APF. The UTT approach is utilized to give the series APF reference voltage signals. Figure 4 depicts the process of generating a reference voltage for each of the series and shunt APF configurations.

A. Generation of the Series APF Reference Voltage Signal

Utilizing Unit Vector Template Generation is an essential step in the process of getting a voltage that is composed of three phases to serve as the reference output for an array APF. A generator of Unit Vector

Templates is used in order to achieve this goal successfully. The three-phases supply voltages (Vsb, Vsa, and Vsc) is used to derive the three-phase in-phase unit templates (Uva, Uvb, and Uvc). In order to construct reference load voltages that are represented by Vlar, Vlbr, and Vlcr, the Unit Vector Template is multiplied by the required highest values (Vt*) of the load voltage.

$V_{lar} = V_t{*} \text{ x } U_{va}$
$V_{lbr} = V_t{*} \text{ x } U_{vb}$
$V_{lcr} = V_t{*} \text{ x } U_{vc}$

B. The Generation of the Shunt APF Reference Current Signal

The shunt APF control technique makes utilization of two PI controllers operating in closed loops. Another of the PI controllers is used to gain the magnitude of the in-phase elements of the reference supply currents (Ispdr), while the first PI controller is utilized to acquire the magnitude of the quadrature elements (Ispqr). In order to set up the first PI controller, measured and reference DC bus voltage measurements are taken from the back-to-back VSI capacitor of the UPQC. In order to execute the second PI controller, detected and reference peak load voltage values (Vt*) are taken.

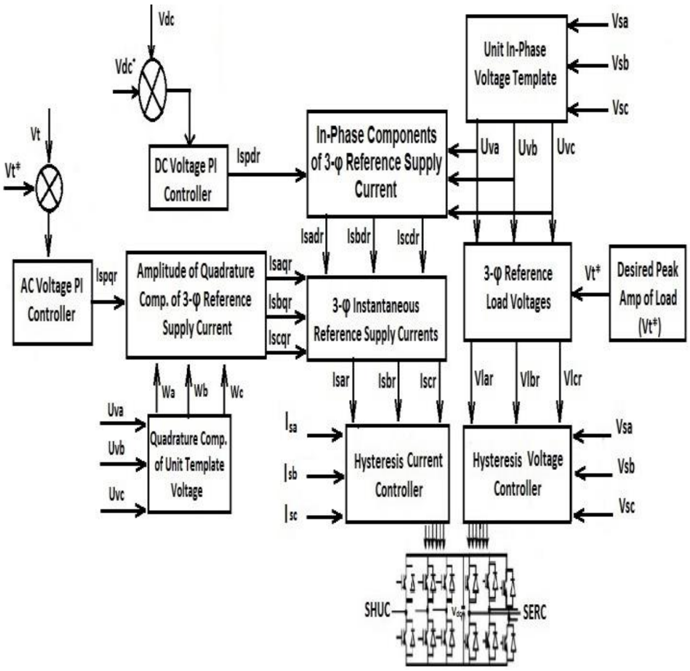

Fig.4. Control Strategy of UPQC

The load voltage is controlled by a pair of distinct components that are an integral component of the reference supply currents for all three phases. Both the voltage at the source as well as the first part of the current that is taken from the point of reference supply are in phase with each other. It is very necessary to provide active power in order to compensate for the load as well as the inefficiencies of the UPQC at the same time. Regarding the second element and the source voltage, there is a connection that may be described as quadrature. This element is in charge of sending reactive power to the load in addition to correcting for voltage control. Its responsibilities also include this. It is necessary to position the supply currents ahead of voltages in order to properly control the voltage. On the other hand, in order to keep the power factor at unity, the supply current need to be moved below the supply voltage. Because of this, it is not possible to meet two demands at the same time, including the control of PCC voltage and the handling of power factor to unity. Both of these needs are incompatible with one another and cannot be satisfied simultaneously. The algorithm for managing the shunt active power element of the UPQC is able to be altered so that it may fulfill either the demand for voltage regulation or the requirement for unity power factor operating while still adhering to the restrictions that were discussed earlier. This allows the UPQC to accomplish both voltage regulation or unity power element performance. The in-phase elements of three-phase reference supply currents are generated by performing the following calculation: multiplied the magnitude of the synchronised elements of reference supply currents (Ispdr) by the synchronized unit current vectors (U_{va}, U_{vb}, and U_{vc}). In-phase reference supply currents are the term that's used to refer to these individual elements. When one combines the magnitudes of the quadrature elements that make up reference supply currents (I_{spqr}) with the quadrature unit current vectors (W_a, W_b, and W_c), one may derive the quadrature elements that make up three-phase reference supply current (I_{saqr}, I_{sbqr}, and I_{scqr}). These components are referred to as the i_{so} phase reference supply currents. This provides one with the quadrature elements of reference supply currents, which are denoted by the symbol "I_{spqr}." The synchronous elements (I_{sadr}, I_{sbdr}, and I_{scdr}) of the shunt APF are the three-phase reference supply currents that are used to ensure that the power factor remains constant throughout operation. On the other hand, the algebraic total of these synchronous and quadrature components results in the production of all three phases of reference supply currents (I_{sar}, I_{sbr}, and i_{scr}) of the shunt APF for the control of voltage. This is because there are components present that are in both the in-phase and quadrature states at the same time.

C. Reference Supply Current In-Phase Components Computation

A PI controller is utilised to apply to the average DC bus voltages of the UPQC and reference VSIs, both of which are coupled in series, in order to estimate the amount of the in-phase element in the reference supply current (I_{spdr}). This is done so that I_{spdr} may be calculated.

$$I_{spdr}(n) = I_{spdr}(n-1)+K_{pd}\{V_{de}(n)-V_{de}(n-1)\}+K_{id}V_{de}(n)$$

Where, V_{dcr} is the reference value of V_{dc} and $V_{de}(n)$ is the difference between the calculated error in V_{dc} and the mean estimate of V_{dc}. The PI controller controlling the DC bus voltages are made up of the proportional and integral gains, denoted by K_{pd} and K_{id}, correspondingly. The procedure to get the in-phase three-phase elements of the reference supply currents is to multiply the PLL-derived synchronous unit current vectors by (I_{spdr}). The equation is used to determine the synchronous reference supply current's amplitude.

$I_{sadr} = I_{spdr} x U_{va}$
$I_{sbdr} = I_{spdr} x U_{vb}$
$I_{scdr} = I_{spdr} x U_{vc}$

D. The Calculation of the Total Reference Currents

The following equation, which represents the algebraic total of the in-phase and quadrature elements, is used to compute immediate three phases reference supply currents:

$I_{sar} = I_{sadr} + I_{saqr}$
$I_{sbr} = I_{sbdr} + I_{sbqr}$

$I_{scr} = I_{scdr} + I_{scqr}$

The reference and sensed supply currents for shunt APF IGBTs are controlled by a carrier-less hysteresis current controller, while the reference and perceived source voltage for series APF IGBTs are controlled by a carrier-less sensitivity voltage controller. Either proportional and integral controllers are used to regulate the reference and detected voltages and current, respectively. This form of regulation replaces the wildly varying currents and voltages of the APF with more stable sources for powering the core components. The outcome is less time spent processing data and fewer sensors needed.

II. RESULT & DISCUSSION

An illustration of a three-wire, three-phase UPQC framework, which is able to be identified in Figure 5, was created with the assistance of the MATLAB/SIMULINK ecosystem. In order to determine whether or not UPQC is effective, power factor correction, load balancing, and the reduction of current and voltage harmonics across a number of different load circumstances are analyzed and measured. This research will focus on a load that consists of a balanced linear delayed power factor load, a resistive load on the dc side of a three phases diode bridge rectifier, and a controlled linear load. All of these components will be combined to form the load. By activating the circuit breaker which is associated with phase b, we were able to create an imbalance in the system. We conduct an analysis to determine if the suggested three-wire, three-phase UPQC management system is effective for controlling sinusoidal supply voltage in addition to distorted main supply.

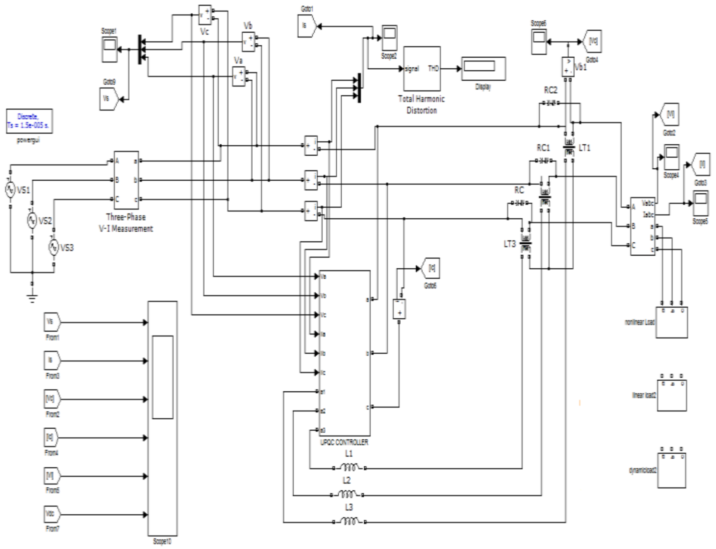

Fig.5. MATLAB design of UPQC

A. Power Factor Correction Performance of UPQC

Figure 6 illustrates the reaction of the UPQC with the controller for the linear lagging power-factor load. At 0.2 seconds, both the series and the shunt APF began their operations. Fig. 6 illustrates that the source current and source voltage in phases 'a' are perfectly phased with respect to one another whenever the R-L load is attached to the UPQC.

B. Performance of UPQC for Voltage and Current Harmonic Moderation

Figure 7 illustrates the reaction of the UPQC for current harmonic reduction with a non-linear load. When the shunt and series APF is activated, the resistive load on the dc side of the rectifiers quickly doubles at t=0.3 seconds, as displayed in Figure 7. This occurs because the APF is connected in series. The source currents have been sinusoidalized and balanced, and their amplitudes have been raised. Even when the load is increased, the UPQC system keeps Vtmn, also known as the peak amplitude, at the value that serves as a reference. The supply currents have a sinusoidal pattern, and their modest leading edge in relation to the supply voltages is noticeable. This is carried out so that the line impedance loss that might be seen in Figure 7 may be accounted for. The voltage generated by UPQC's dc bus is controlled to remain at its reference value, and this eventually leads to the formation of a dc bus that is capable of sustaining itself. The efficiency of the control strategy for current harmonic suppression is assessed by switching on a three-phase diode bridge rectifier having a resistive load on the dc side for 0.3 seconds. This test is performed to measure the efficacy of the control procedure. This is done in order to assess the efficacy of the algorithm. Because of this, there is a distortion in the load current. It has been shown that supply currents are evenly distributed, sinusoidal in shape, and in phase relative to the voltages even though the voltage used for utility purposes is not sinusoidal. This is because supply currents are proportional to the voltages. This is the case even when the utility voltage is not sinusoidal. The total harmonic distortion (THD) of the source current has dropped from 29.26% to 4.69%, as illustrated in figures 8 and 9. The harmonic spectra of the source current are shown with and without correction in Figures 8 and 9, respectively.

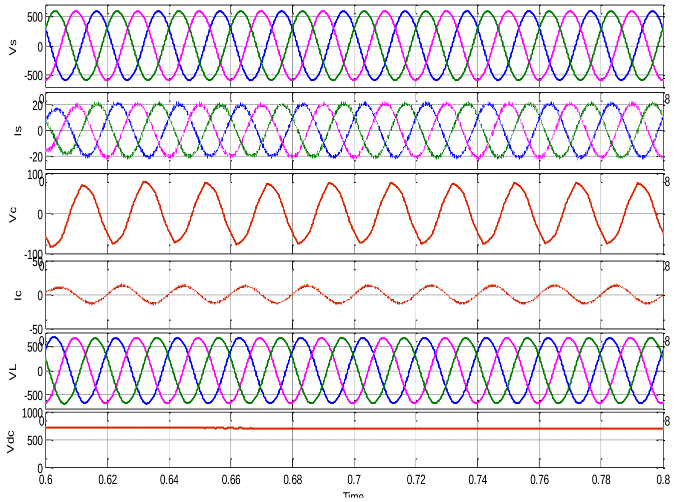

Fig.6 Efficiency of the UPQC with regard to Power Factor Correction

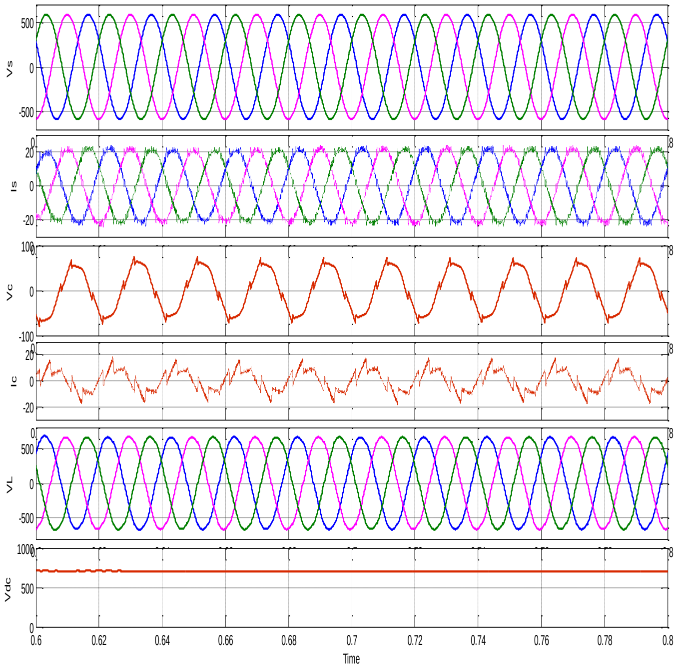

Fig.7 Evaluation of the UPQC for the Purpose of Current Harmonic Mitigation

C. The effectiveness of UPQC in terms of load balancing

At 0.2 seconds, both the series and the shunt APF began their operations. At the time equal to half a second, the load is converted from three phases to two phases in order to produce an unbalanced load. The source currents remain balanced following that the UPQC has compensated for the unbalanced load, which means they are in phase to the source voltages. Figure 10 further demonstrates that when a load that is not balanced is run, the dc voltage increases and then, after the load is balanced, it returns to its previous steady state value. This phenomenon can be seen when an unbalanced load is operated. On the direct current (dc) side of the circuit, the response of UPQC for the balance of loads is displayed when a three-phase diode bridge rectifier is paired with a resistive load. The dc portion of the circuit is where this action will take place. Figure 11 demonstrates that the supply currents are sinusoidal and have a balanced distribution. Additionally, they are shown to be in phase with the voltages shown in the diagram.

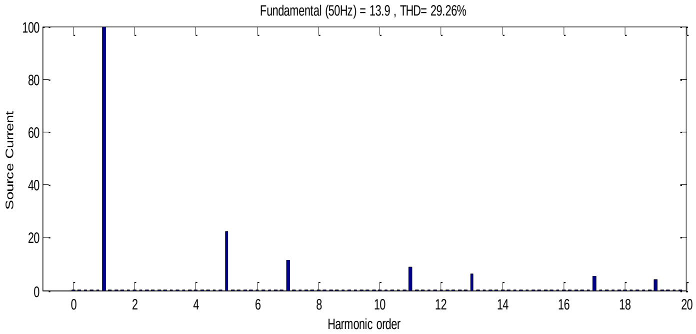

Fig.8. Source Current without compensation

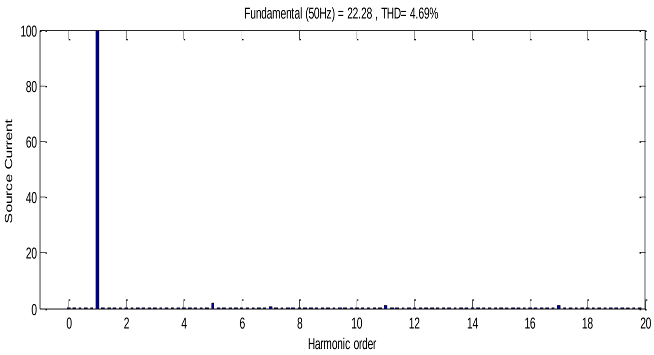

Fig.9. Source Current with compensation

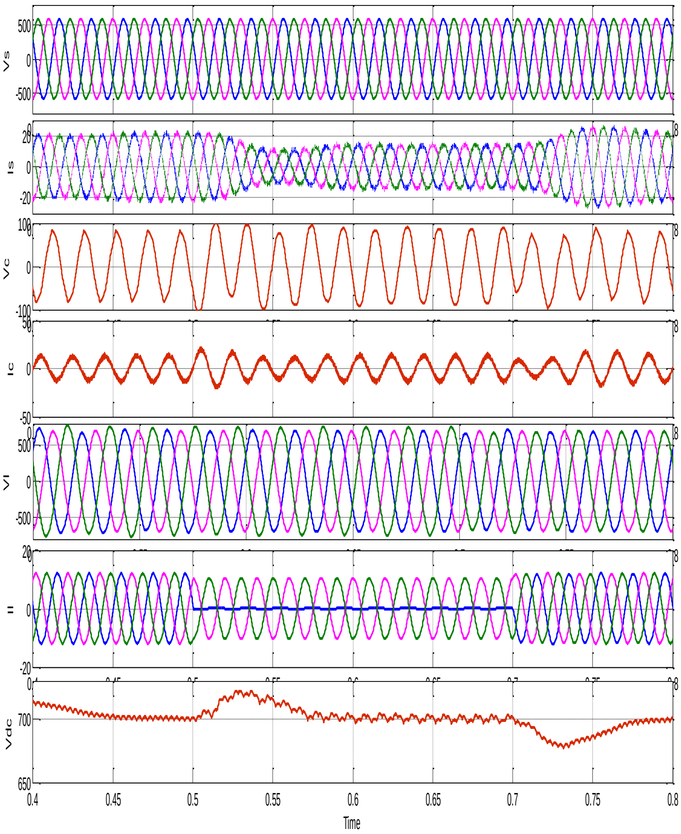

Fig.10. Performance of UPQC for Linear-load balancing

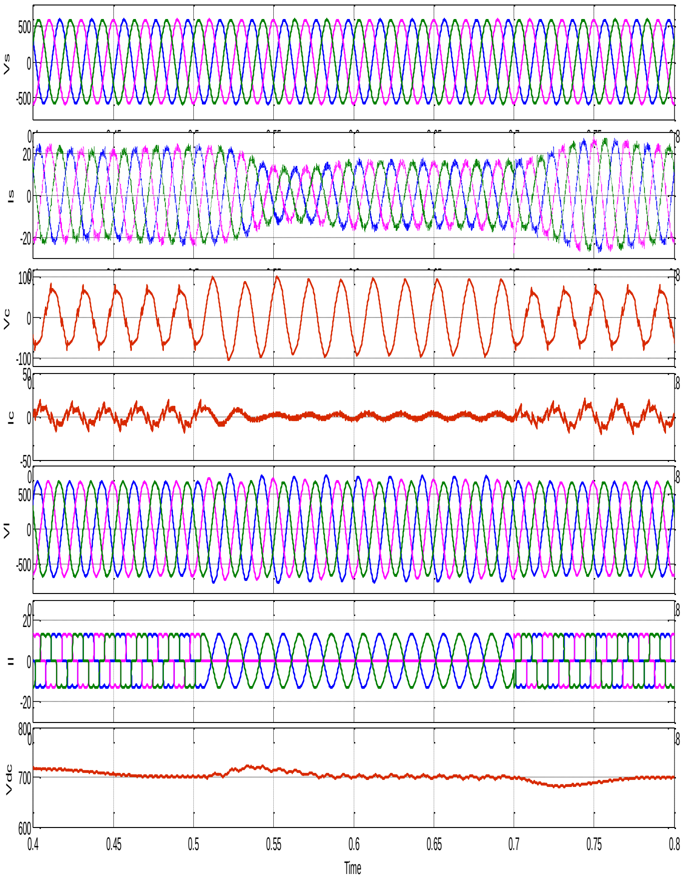

Fig.11. Load Balancing for Non-Linear Load

III. CONCLUSION

Software implementation in MATLAB/SIMULINK has successfully achieved the stated goals. The effectiveness of UPQC has been examined in a variety of real-world contexts. A setup of UPQC that uses UTT-based control has shown that it functions well. The effectiveness of the UPQC has been examined in terms of a number of different enhancements to power quality, including load balancing, power factor correction, reduction of harmonics (both voltage and current), voltage dip, and dc voltage control. Those are only some of the many potential enhancements to the power quality that were recently investigated. The source current now has a THD of 4.69%, which is a significant improvement from its previous value of 29.26%. under addition, it was found that UPQC's performance under unpredictable circumstances was satisfactory. This was verified after an investigation. Future work on this thesis topic will focus on developing a UPQC hardware model and implementing it in a variety of UPQC topologies in an effort to reduce the amount of space required for the UPQC controller as well as its associated cost.

IV. APPENDIX

[1] Voltage at the supply: 415 volts RMS at 50 hertz.

[2] The impedance of the supply is 50 H at 0.01 ohms.

[3] The value of the DC link capacitance is 4000 uF.

[4] 700 volts is the DC link voltage.

[5] Parameters of the ripple filter are as follows: 0.01, 0.5mH; 0.1, 0.5mH; and 1.4F.

[6] Transformer with a rating of 1KVA and 100V/100V.

[7] Inductive load equal to 1.25 kvar for 5 kW of linear load.

Rectifier for a single phase load that is not linear load R=50 ohms is the load on the dc side.

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